High-Information-Content Color 16.3"-Desktop-AMLCD with 15.7 Million a-Si:H TFTs

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1. Abstract

A direct-view active matrix display with the highest information content ever shown has been developed using cost effective a-Si:H-TFT technology. This 16.3" diagonal QSXGA (Quad SXGA) display incorporates 2560x3 columns (RGB color stripes) and 2048 rows. The subpixel size is 42μm(h)x126μm(v) which is equivalent to a full color resolution of 200ppi (pixels per inch).

2. Introduction

Active matrix displays based on amorphous silicon technology have become the dominant technology used for flat panel displays in notebooks. Recently active matrix displays are also beginning to penetrate into the desktop monitor market due to the advantages of active matrix technology compared to CRTs, such as flickerfree images, no radiation, low power consumption and light weight. In the work reported here we show that LCDs can go well beyond the capability of CRTs in resolution and information content.

Today's constantly increasing processor clock rates, more complex operating systems higher resolution graphic and multimedia applications created a desire for high information content displays. Color CRT displays are limited to approximately 100ppi for cost effective tube fabrication. Therefore the same QSXGA display in CRT technology would require a diagonal of 32.6" which would be too large and heavy for desktop applications in the workplace.

Despite further improvements in low-temperature polysilicon technology and the latest predictions for its applications [1], we show that a-Si:H is capable of building the highest information content desktop displays to date and that polysilicon is not required for these displays. Furthermore for these types of desktop displays the a-Si:H technology offers the lowest cost active matrix.

The technology transition from a 12.1"-SVGA to the 16.3"-QSXGA can be compared to the transition from a dot matrix printer to today's laser printers.

3. Design and Feasibility

The C_s-on-gate design of two subpixels is shown in Figure 1 for the 6-mask I-stopper process used. For 6μsec gate pulse width the design requires the gate lines to be driven from

both ends and it requires a minimum TFT mobility of 0.4 cm^2/Vs. The W/L of the pixel TFT is 10μm/6μm and the data line width is 7μm.
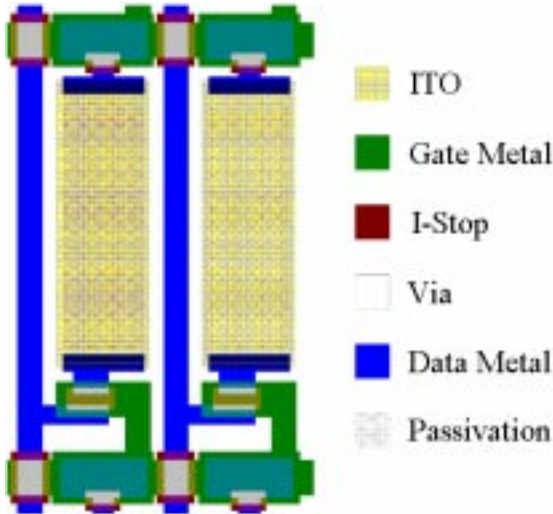

Figure 1   Layout of the QSXGA subpixels

With the assumptions above the feasibility limits are determined by the conductivity of lines in the array, the charge capability of the TFTs for 6-bit graylevel and the capacitance ratio between parasitic coupling capacitors, liquid crystal capacitor and storage capacitor.

The conductivity of the gate lines is more critical than that of the data lines [2]. Figure 2 is a feasibility chart for different display types and is derived from prior papers [3][4]. The dashed lines show the fixed relationship between diagonal and resolution for XGA, SXGA, QXGA and QSXGA displays. In 1996 a 150 ppi 10.5"-SXGA notebook display was published[5][7]. The crossover point between the gate metal material lines and the display type lines marks the limit of feasibility.

For good yield in fabrication a study of the sensitivity of the design towards layer to layer overlay issues and towards etch homogenity issues has been carried out.
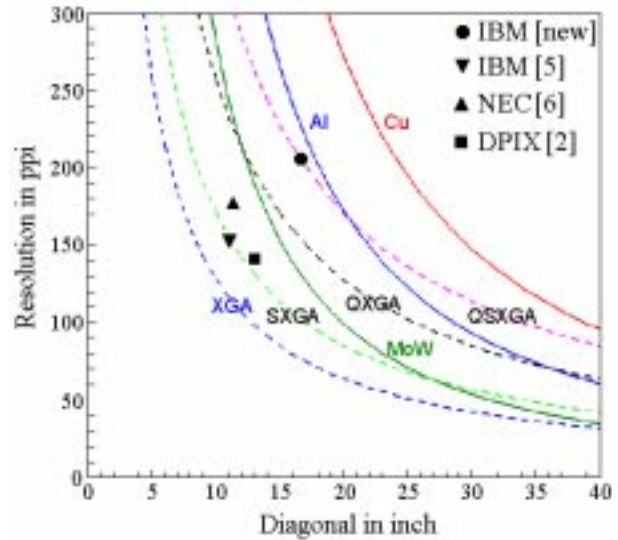

Figure 2   Feasibility of High Resolution AMLCDs

4. Module Fabrication Process

The 16.3"-QSXGA active matrix array has has been fabricated on 381mm x 381mm Corning 1737 substrates using a similar process as described in [5]. Processing data from the 150 ppi SXGA prototype in [5] has been used as feedback for the design of this QSXGA prototype to give an optimum processing window. Figure 3 shows the 6-mask process flow.

The sputtered ITO is wet etched by hydrochloric/nitric acid etch after patterning photoresist using the 1st mask. The sputtered Al alloy is wet etched after patterning photoresist with the 2nd mask. Both Al-Cu and Al-Y have been successfully used. After the deposition of the trilayer SiN$_x$/a-Si:H/SiN$_x$ by PECVD, as gate insulator, semiconductor and I-stop respectively, the I-stop SiN$_x$ is wet etched after patterning photoresist with the 3rd mask. The via openings are formed in the 4th mask step after deposition of n+ a-Si using a RIE etch process with optimized taper. After

sputtering Mo/Al/Mo as data metal it is patterned using the 5th mask followed by a RIE etch of the remaining n+ a-Si between the data metal gaps. The SiN_x passivation layer is deposited by PECVD and patterned using the 6th mask. An overlay error less than 1μm from layer to layer during processing was assured.
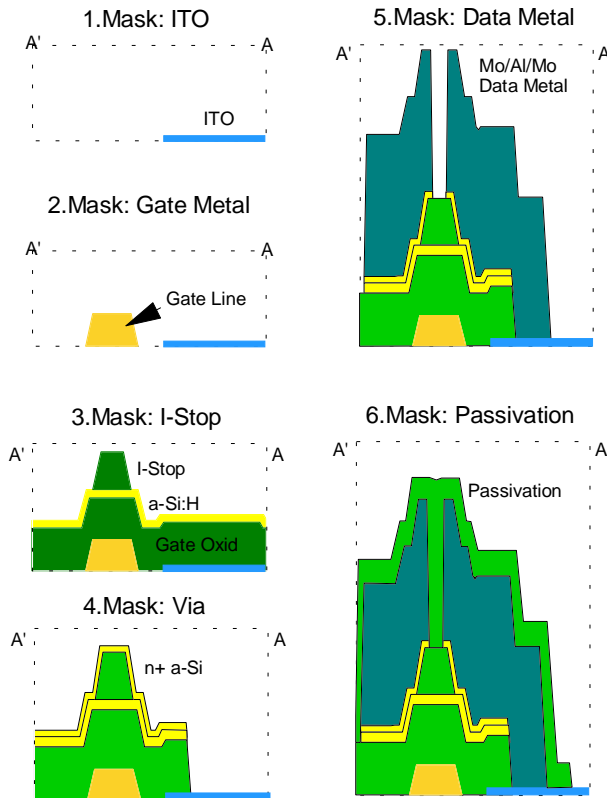

Figure 3   6-mask Process Steps

During the cell assembly process an alignment error of less than 1μm between array substrate and color filter substrate is typical.

5. Driving Electronics

At 60Hz frame rate the data stream flow for the QSXGA display would be at least 943Mbyte/sec, excluding blanking periods. To cut down this data transfer rate the display is driven as four vertical stripes in parallel. Each of the stripes is driven by four 6-bit 240-output column signal drivers on the top and bottom. The gate lines are driven from both ends by 14 gate driver chips with 154 outputs each. The panel can be driven in dot inversion or column inversion. Figure 4 shows a photograph of the color 16.3"-QSXGA-display.

Figure 4 Photograph of the QSXGA display

Figure 5 shows a closeup of the 200ppi display compared to a 12.1"-SVGA 83ppi display. Readibility of Times New Roman text displayed on screen at 10pt has been improved near to the quality of print on paper.
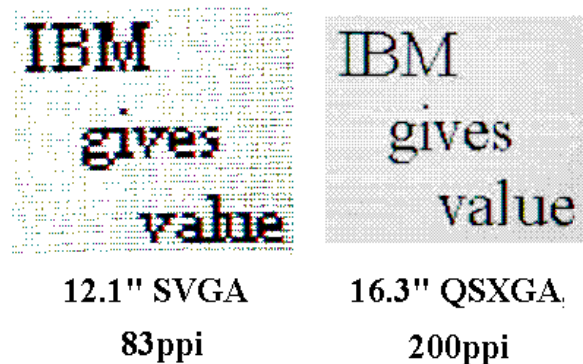

Figure 5   Images of 10pts high text

Table 1 shows the specifications of the QSXGA display module.

Columns x Rows	7680 x 2048
Subpixel Size	42μm x 126μm
Subpixel Count	15,728,640
Array Diagonal	16.3 inch
Spatial Resolution	200 pixel per inch
# of Colors	262,144
Aperture Ratio	27.3%
Gate Metalurgy	Al-alloy
Frame Rate	60Hz
Gate Pulse Width	6μsec
Luminance	230 cd/m^2
LC Mode	TN, normally white
Contrast Ratio	150:1
Backlight Power	42W
Total Power	<75W (dot inversion)

Table 1   Specifications of the QSXGA-TFT-AMLCD prototype

The power consumption of this QSXGA display is at least a factor two smaller compared to a 17"-CRT in SXGA mode.

6. Summary

An active matrix desktop display (QSXGA) with the highest information content and with the highest color pixel resolution (200ppi) to date has been built successfully using a-Si:H TFT technology with Al alloy gate lines. Due to the system design this 16.3"-QSXGA display runs Windows NT and is multimedia capable at 60Hz frame rate. A prototype will be shown at the author's interview.

7. Acknowledgements

The design and fabrication of the QSXGA displays are a result of teamwork involving scientists and engineers from IBM Research in Yorktown Heights (USA) and the IBM Display Business Unit in Yamato/Yasu (Japan). The high quality color filters were fabricated by Optical Imaging Systems (OIS) according to IBM's design specifications.

8. References

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